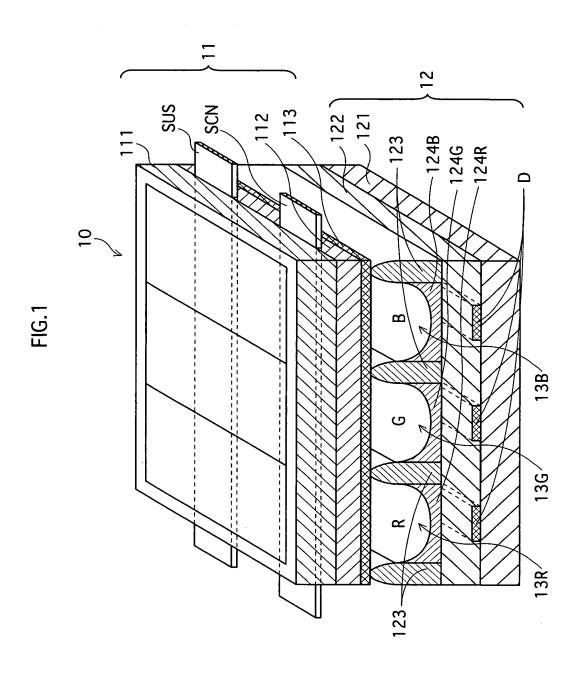
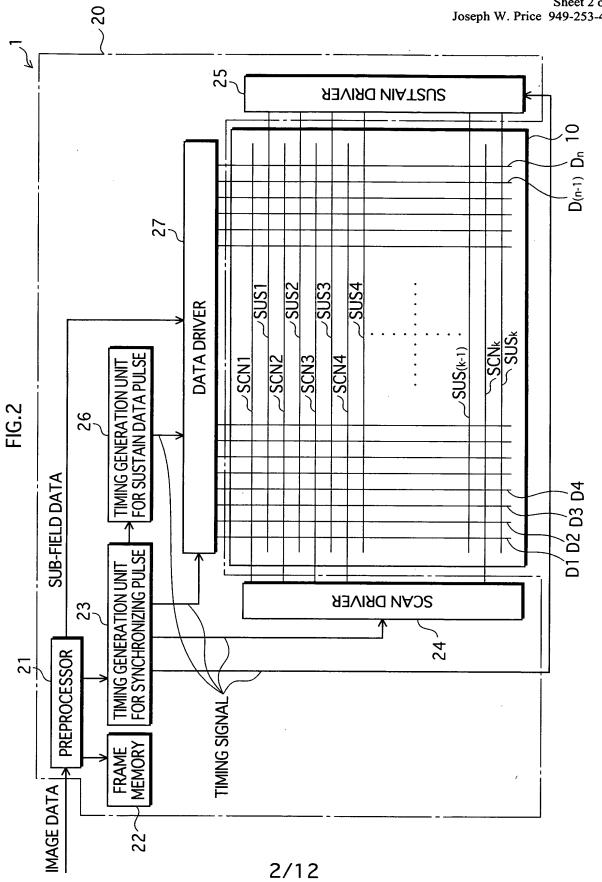
10/533840 Shinichiro Hashimoto et al. 92478-2700 Sheet 1 of 12 Joseph W. Price 949-253-4920

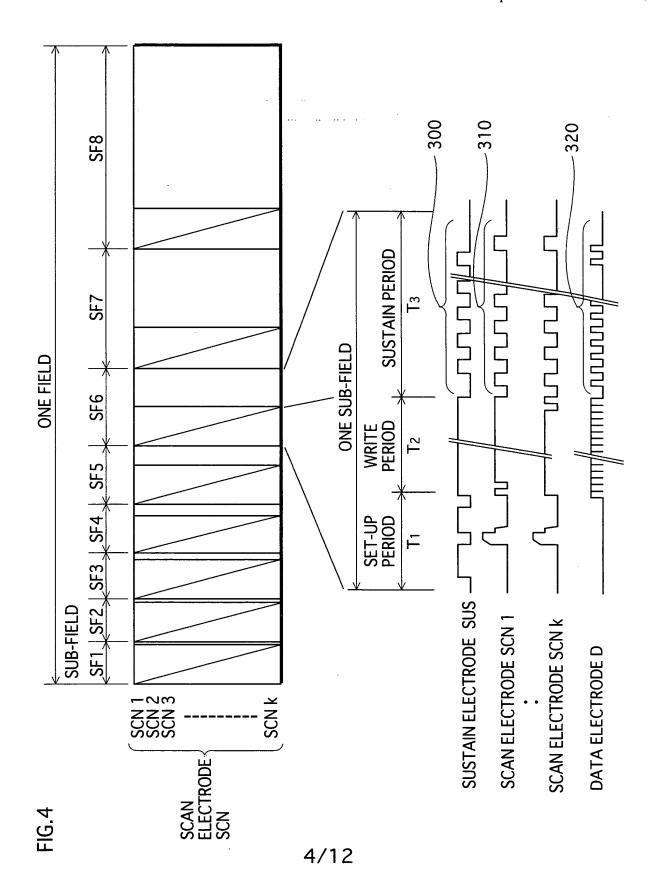


10/533840 Shinichiro Hashimoto et al. 92478-2700 Sheet 2 of 12 Joseph W. Price 949-253-4920

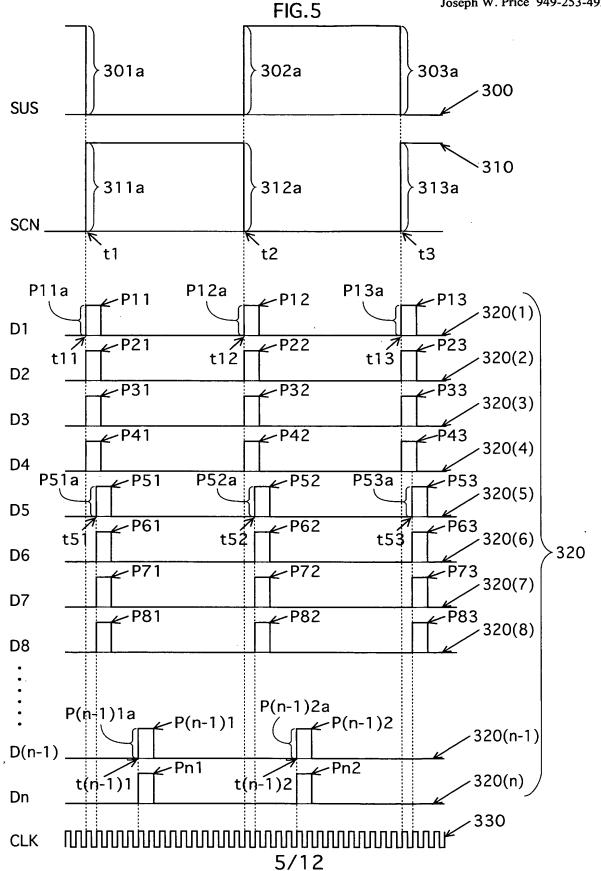


Shinichiro Hashimoto et al. 92478-2700 Sheet 3 of 12 Joseph W. Price 949-253-4920 0 D(n-3) D(n-1) D(n-2) DDRIVING **CIRCUIT N** Sig.m SIRCUIT 3 DRIVING FOR SUSTAIN DATA PULSE TIMING GENERATION UNIT FIG.3 CIRCUIT 2 DRIVING SUB-FIELD DATA DRIVING CIRCUIT Sig.3 \ Sig.2 \ \ Sig.1 FOR SYNCHRONIZING PULSE **TIMING GENERATION UNIT** TO SCAN DRIVER AND SUSTAIN DRIVER → PREPROCESSOR TIMING SIGNAL TO FRAME MEMORY 3/12

Shinichiro Hashimoto et al. 92478-2700 Sheet 4 of 12 Joseph W. Price 949-253-4920

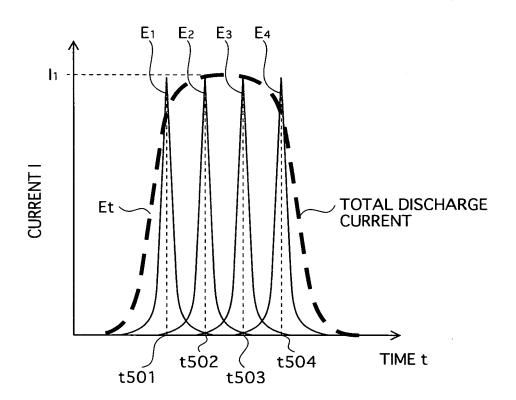


Shinichiro Hashimoto et al. 92478-2700 Sheet 5 of 12 Joseph W. Price 949-253-4920

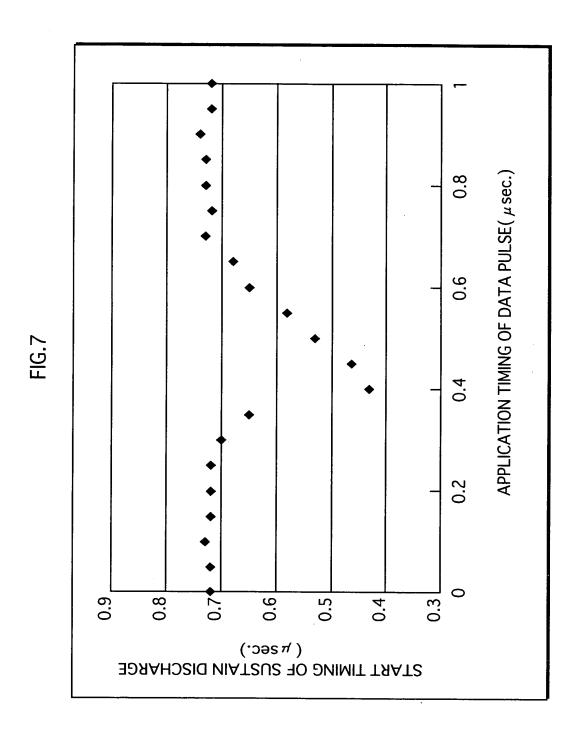


Shinichiro Hashimoto et al. 92478-2700 Sheet 6 of 12 Joseph W. Price 949-253-4920

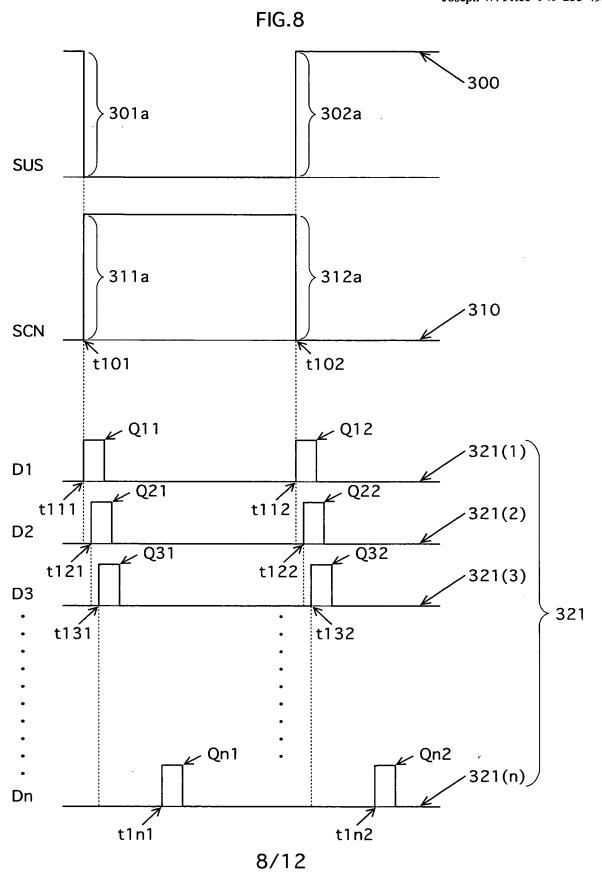
FIG.6



Shinichiro Hashimoto et al. 92478-2700 Sheet 7 of 12 Joseph W. Price 949-253-4920

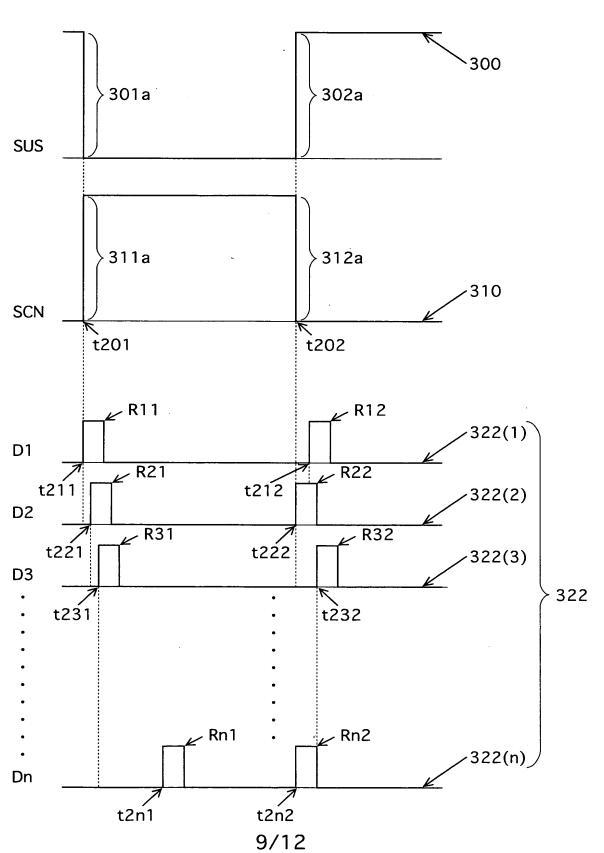


Shinichiro Hashimoto et al. 92478-2700 Sheet 8 of 12 Joseph W. Price 949-253-4920

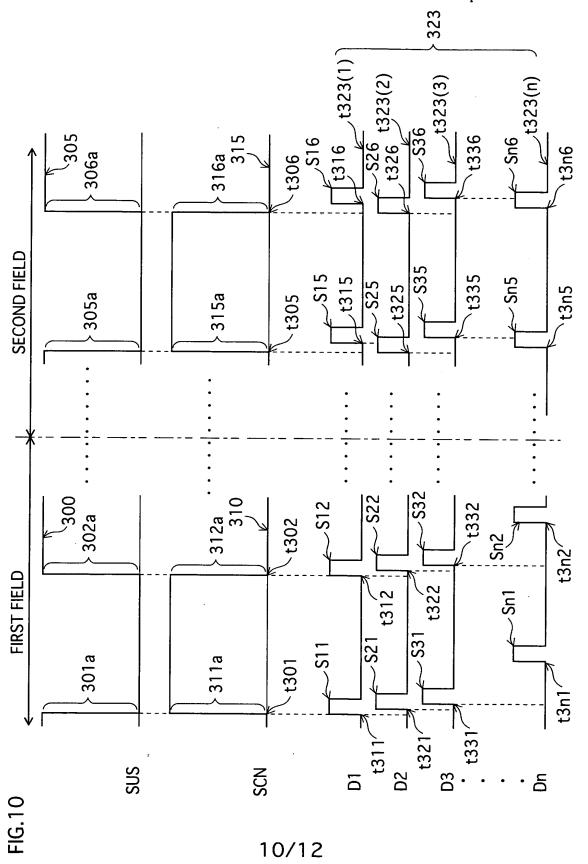


Shinichiro Hashimoto et al. 92478-2700 Sheet 9 of 12 Joseph W. Price 949-253-4920





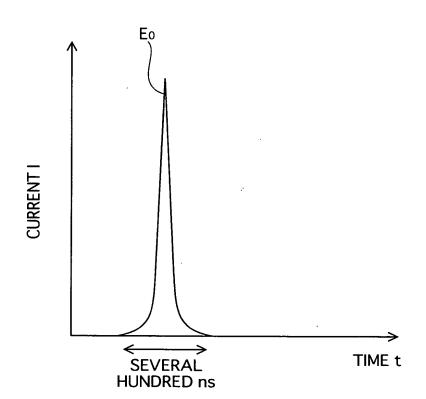
Shinichiro Hashimoto et al. 92478-2700 Sheet 10 of 12 Joseph W. Price 949-253-4920



10/533840

Shinichiro Hashimoto et al. 92478-2700 Sheet 11 of 12 Joseph W. Price 949-253-4920

FIG.11



10/533840

Shinichiro Hashimoto et al. 92478-2700 Sheet 12 of 12 Joseph W. Price 949-253-4920

FIG.12

